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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,407	01/09/2004	Michael Bernhard Sommer	INF-126	6375

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/753,407	SOMMER, MICHAEL BERNHARD	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *7-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10 and 11* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5-19-04, 10-20-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed April 18, 2005.

Election/Restrictions

Applicant's election without traverse of claims 1-6 and 10-12 in the reply filed on April 18, 2005 is acknowledged.

Oath/Declaration

The prior Foreign application number is stated as "103 00 6**78**.7" but should have been 103 00 6**87**.1 in the declaration.

Drawings

Figures 1 and 2A-2B should be designated by a legend such as --**Prior Art**-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: **G1** in Figure 2A. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Kimura et al. (5,323,043).

In regard to claim 1, Kimura et al. teach a semiconductor chip comprising: a plurality of wells 5' & 5 of a first conduction type, each well formed in a substrate 1 and

containing a first set of active components and a first set of contacts 10 & 17 associated with the first set of active components; and a plurality of wells 2 & 3 of a second conduction type, each well formed in a substrate 1 and containing a second set of active components and a second set of contacts 10 & 16 associated with the active components, wherein the wells 5' & 5 of the first conduction type share a mutually adjoining boundary with the wells 2 & 3 of the second conduction type, wherein the first set of contacts 11 & 17 and a second set of contacts 10 & 16 lie in region near the mutually adjoining boundary, and wherein the active components lie further away from the mutually adjoining boundary than do the first 11 & 17 and second 10 & 16 set of contacts (Figure 3, column 3, lines 34-55).

In regard to claim 3, Kimura et al. teach the circuit layout structures not mirror-symmetrical with respect to a centerline therein (Figure 3, column 3, lines 34-55).

In regard to claim 5, Kimura et al. teach the wells 5' & 5 of the first conduction type are p-type, and include n-channel FETs fabricated thereon, and wherein the wells 2 & 3 of the second conduction type are n-type, and include p-channel FETs fabricated thereon (Figure 3, column 3, lines 34-55).

In regard to claim 10, Kimura et al. teach a chip architecture comprising: a plurality of pairs of wells, each pair including an n-type well 2 & 3 adjacent to a p-type well 5' & 5, wherein a border region is defined along an edge where each n-well 2 & 3 and p-well 5' & 5 are mutually adjacent; a set of contacts within each well arranged to lie within the border region; and a set of active components within each well arranged to lie outside the border region (Figure 3, column 3, lines 34-55).

In regard to claim 11, Kimura et al. teach the arrangement of the pairs of wells 2, 3, 5' & 5 is such that there is no mirror symmetry of the well location with respect to a line through the center of the chip (Figure 3, column 3, lines 34-55).

In regard to preamble of claim 1 (a semiconductor memory chip) and claim 10 (a DRAM memory chip architecture), the claim preamble must be read in the context of the entire claim. The determination of whether preamble recitations are structural limitations or mere statements of purpose or use "can be resolved only on review of the entirety of the [record] to gain an understanding of what the inventors actually invented and intended to encompass by the claim." Corning Glass Works, 868 F.2d at 1257, 9 USPQ2d at 1966. If the body of a claim fully and intrinsically sets forth all of the limitations of the claimed invention, and the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction. Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999). See also Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. (5,323,043) as applied to claims 1, 3, 5 and 10-11 above, and further in view of Sawada et al. (5,726,475).

Kimura et al. teach all mentioned in the rejection above.

Such as in regard to claim 4, Kimura et al. teach the circuit layout structures not mirror-symmetrical with respect to a center line therein (Figure 3, column 3, lines 34-55); and in regard to claim 6, Kimura et al. teach the wells 5' & 5 of the first conduction type are p-type, and include n-channel FETs fabricated thereon, and wherein the wells 2 & 3 of the second conduction type are n-type, and include p-channel FETs fabricated thereon (Figure 3, column 3, lines 34-55).

However, Kimura et al. fail to teach a memory chip comprising a DRAM chip.

In regard to claim 2, Sawada et al. teach a memory chip comprising a DRAM chip (Figure 3M, column 4, lines 6-10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify semiconductor chip structure as taught by Kimura et al. with the semiconductor chip having a memory chip comprising a DRAM chip as taught by Sawada et al. to significantly improve the performance and characteristics of the semiconductor device (column 8, lines 37-43).

Allowable Subject Matter

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor chip structures:

Kanehira et al. (US 6,212,671 B1) Karasawa et al. (US 6,791,147 B1)

Lines (US 6,703,670 B1) Lotfi et al. (US 2002/0175366 A1)

Maeda et al. (US 2003/0042548 A1) Nishida et al. (US 6,586,807 B2)

Omoto et al. (5,043,788) Shibata et al. (US 2004/0026743 A1)

Takahashi et al. (5,311,048).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
May 10, 2005